REMARKS

Claims 1 - 19 are pending. Claims 1, 2, 4-10, 12-14 and 16-19 stand rejected. Claims 3, 11 and 15 are allowed.

Claims 1-14 and 16-19 have been amended and claims 20-24 have been added. No new matter has been added.

Claim 8 stands rejected under 35 USC 102(b) as being anticipated by Carmean (U.S. Patent No. 5,669,003). It is the examiner's position that Carmean disclosed each and every element recited in the claims.

Applicant respectfully disagrees with, and explicitly traverses the examiner's reason for rejecting the claims. However, in order to advance the prosecution of this application, applicant has elected to amend the claims to more clearly state the invention. More specifically, applicant has elected to amend independent claim 8 to more clearly state the invention, which now recites:

> 1. A data processing unit having access to a memory belonging to the data processing unit situated in a switched-off mode, wherein the memory belonging to the data processing unit is accessible to a second data processing unit having a second memory unit of its own.

No new matter has been added. Support for the amendments may be found on page 4, lines 3-4, which state in part, "[i]f the microprocessor 10 is switched off in the reduced power mode, the whole part of the memory 15 that is assigned to the microprocessor 10 becomes available to the video controller 17."

Carmean, on the other hand, discloses a method for maintaining cache coherency while minimizing power consumption. The method includes operating a first processor in a reduced power mode ..[of which] ... certain portion of the internal logic in the first processor remain clocked so that the first processor continues to monitor transactions of the system bus." (See Abstract). Carmean fails to disclose that the first processor is switched-off because the method of Carmean requires that the first processor continue some minimal operation to be responsive to a request by the second processor.

It is well recognized that to constitute a rejection pursuant to 35 USC 102, i.e., anticipation, all material elements recited in a claim must be found in one unit of prior art. For the reason shown, Carmean cannot be said to anticipate the present invention, because Carmean fails to disclose each and every element recited in claim 8.

Having shown that Carmean fails to disclose each and every element recited in the claim, applicant submits that the reason for the examiner's rejection of the claim has been overcome and the rejection can no longer be sustained. Applicant respectfully requests entry of the amendment, reconsideration, withdrawal of the rejection and allowance of the claim.

Claims 1-2, 4-10, 12-14 and 16-19 stand rejected under 35 USC 103(a) as being unpatentable over Conary (USP No. 5,481,731) in view of Carmean.

Applicant respectfully disagrees with, and explicitly traverses, the examiner's reasons for rejecting the claims. A claimed invention is prima facie obvious when three basic criteria are met. First, there must be some suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the teachings therein. Second, there must be a reasonable expectation of success. And, third, the prior art reference or combined references must teach or suggest **all** the claim limitations.

With regard to claim 1, which is typical of the independent claims 8 and 13, this claim recites:

> 1. A data processing system which is adapted to function in a reduced-power mode, comprising:
>
> a first data processing unit that has access to a memory belonging to the first data processing unit; and,
>
> a second data processing unit having its own memory, said second data processing unit having access to the memory belonging to the first data processing unit, wherein the first data processing unit is **arranged for offering** the second data processing access to the memory belonging to the first data processing unit in a reduce-power mode of the data processing system so that the second data processing unit utilizes the memory belonging to the first data processing unit instead of its own memory.

Conary discloses a method and system for allowing a processor to invalidate an individual line of its internal cache while in a non-clocked low power state. Conary teaches that the processor monitors the memory and when a change is written into the memory by another device, the processor is powered-up momentarily to alter a cache memory to correspond to the change made to the memory. However, Conary fails to teach or suggest that the first processor is "arranged for offering" the second device access to the memory. Rather, in the system of Conary all the devices have access to the memory. (See Figure 1 and col. 19, lines 60-65, which state, in part, "the processor includes an internal cache, when powered down, other devices ... may be accessing the external memory.").

Further the devices referred to by Conary are passive device, e.g., keyboard, cursor control device, etc., that are suitable to access the memory whether the processor is in a low-power mode or not. These devices also are not comparable to "a second data processing unit having its own memory," as is recited in the claim.

Carmean, as noted above, discloses a method for maintaining cache coherency while minimizing power consumption. The method includes operating a first processor in a reduced power mode ..[of which] certain portion of the internal logic in the first processor remain clocked so that the first processor continues to monitor transactions of the system bus."

Neither Conary nor Carmean, individually or in combination, teach or suggest all the elements recited in the above referred-to claims. From the teachings of Conary and Carmean, even if combined, one would not be motivate to develop a system wherein "the first data processing unit is arranged for offering the second data processing access to the memory belonging to the first data processing unit." In fact, one would not be motivated to combine the teaching of Conary and Carmean to develop the novel features claimed, because Conary teaches powering-up the reduced-power processor to alter cache memory when the main memory is accessed by another device and Carmean teaches that the processor is responsive to an access when a request for access is made. Hence, neither reference would motivate one skilled in the art to offer memory to a second processor when the first processor enters a low-power state, as is claimed

Having shown that the combination of Conary and Carmean fails to teach or suggest all the elements recited in claim 1, applicant submits that the reason for the examiner's rejection has been overcome and the rejection can no longer be sustained. Applicant respectfully requests entry of the amendments, reconsideration, withdrawal of the rejection and allowance of the claims.

ith regard to claims 8 and 13, these claims recite data processing units similar to that recited in claim 1 and include claim language similar to the amended language in claim 1. The examiner rejected these claims for the same reason used in rejecting claim 1. Thus, the applicant's remarks made in response to the examiner's rejection of claim 1 are also applicable in response to the examiner's rejection of claims 8 and 13. In view of the amendments made to claims 8 and 13 and for the remarks made with regard to the rejection of claim 1, which are repeated herein in response to the rejection of the above referred to claim, applicant submits that the examiner's reason for rejecting these claims has been overcome and the rejection can no longer be sustained. Applicant respectfully requests entry of the amendment, reconsideration, withdrawal of the rejection and allowance of the claims.

With regard to claims 2, 4-10, 12-14 and 16-19, these claims ultimately depend from claims 1, and 13 which has been shown to include subject matter not disclosed in, and, hence, allowable over the cited reference. Accordingly, claims 2, 4-10, 12-14 and 16-19 are also allowable by virtue of their dependence from an allowable base claim. Applicant respectfully request reconsideration, withdrawal of the rejection and allowance of the claim.

New claims 20-24 have been added to recite other embodiments of the present invention. No new matter has been added. Support for the new amendments may be found on page 4, lines 28-30, which state, in part "[t]he microprocessor 30 is not switched off in some systems, but needs to execute only a minimum set of tasks. ... the microprocessor needs to have only a small portion of the memory ... By allowing the video controller to make use of the unused part of the memory." Also, see the description with regard to Figure 4 on pages 4 and 5.

Applicant, through his attorney, wishes to thank the examiner for his indication of allowable subject matter in claim 3, 11 and 15. However, in view of the amendments made to the claims and for the remarks made herein, applicant believes that all the claims are allowable.

Applicant further submits that the amendments made to the claim were made to more clearly describe the subject matter the applicant regards as his invention and to correct errors in form. The amendments were not necessarily made to overcome the references cited. Accordingly, the amendments made are not related to patentability and do not alter or limit the substance of the subject matter claimed.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Should any unresolved issues remain that the examiner believes may be resolved via a telephone call, the examiner is invited to call Applicant's attorney at the telephone number below.

No fees are believed necessary for the filing of this Amendment and Response.

Respectfully submitted,
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